PRODUCT SPECIFICATION

MODEL: MTF035DV49A-V1

<◇> PRELIMINARY SPECIFICATION

<◆> APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED
LCM研发 2021.08.06 YYL	LCM研发 2021.08.06 YGP	LCM研发 2021.08.06 Edward

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Record of Revision

Rev	Issued Date	Description	Editor
V1	2021-08-06	Preliminary Specification Release	

1 General Specifications

Feature		Spec
Display Spec.	Size	3.54 inch
	Resolution	640(RGB) x 960
	Technology Type	a-Si
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(mm)	26(H)x3x78x(v)
	Display Mode	Normally Black
	LCM Luminance	400 Cd/m2
	Viewing Direction	ALL
Mechanical Characteristics	Module (W x H x D) (mm)	54.56x82.84x2.25±0.15mm
	Active Area(mm)	49.92x74.88mm
	Matching Connection Type	FPC
Electrical Characteristics	LED Numbers	6LEDs
	TFT Interface	MIPI
	Display color	16.7M
	LCD Driver IC	ST7703

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: /S0002

Note 3: LCM weight tolerance: 5

2 Input/Output Terminals

Pin No.	Symbol	Function description
1	LCD ID	NC.
2	NC	NC.
3	LEDA	LED anode.
4	LEDA	LED anode.
5	NC	NC.
6	LEDK	LED cathode.
7	LEDK	LED cathode.
8	NC	NC.
9	GND	System power ground.
10	GND	System power ground.
11	CLKN	MIPI_DSI clock Lane negative-end input pin.
12	CLKP	MIPI_DSI clock Lane positive-end input pin.
13	GND	System power ground.
14	DATA0N	MIPI_DSI data Lane0 negative-end input/output pin.
15	DATA0P	MIPI_DSI data Lane0 positive-end input/output pin.
16	GND	System power ground.
17	DATA1N	MIPI_DSI data Lane1 negative-end input/output pin.
18	DATA1P	MIPI_DSI data Lane1 positive-end input/output pin.
19	GND	System power ground.
20	GND	System power ground.
21	TE	Tearing effect output pin.
22	GND	System power ground.
23	GND	System power ground.
24	LCD RST	Chip reset signal pin.
25	NC	System power ground.
26	VCC	System power supply.(Typ.:5.5V)
27	VCC	System power supply.(Typ.:5.5V)
28	NC	NC
29	IOVCC	Power supply for interface pins.(Typ.:1.8V)
30	IOVCC	Power supply for interface pins.(Typ.:1.8V)

3 Absolute Maximum Ratings

(Ta=25℃)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage for Analog		VSP	5.0	5.5	6.0	V	
		VSN	-5.0	-5.5	-6.0	V	
Power supply voltage for Logic		IOVCC	1.70	1.80	1.90	V	
Input signal voltage (RES)		V_{IL}	0	-	0.3* IOVCC	V	XRES
		V_{IH}	0.7* IOVCC	-	IOVCC	V	
Onput signal voltage (TE)		V_{OL}	0	-	0.2* IOVCC	V	TE
		V_{OH}	0.8* IOVCC	-	IOVCC	V	
Input signal voltage (DSI)	Low level	$V_{IL(DSI)}$	-50	-	550	mV	Low power receiver
	High level	$V_{IH(DSI)}$	880	-	1350	mV	
	Input voltage	V_{CMRX}	70	-	-	mV	High speed receiver
	Differential input low threshold	V_{IDTL}	-70	-	-	mV	
	Differential input high threshold	V_{IDTH}	-	-	70	mV	

Note: The recommended operating condition refers to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be with the absolute maximum ratings. Accordingly, please make sure that the module is used within this range

4 Electrical Characteristics

4.1 LCD characteristics

GND 0V,Ta 25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		IOVCC	1.70	1.8	1.9	V	
Power Supply Voltage		VSP(+5V)	5.0	5.5	6.0	V	
Power Supply Voltage		VSN(-5V)	-5.0	-5.5	-6.0		
Input Signal Voltage	High Level	VIH	0.7*IOVCC	-	IOVCC	V	
	Low Level	VIL	0	-	0.3*IOVCC	V	

Table 4.1 LCD module electrical characteristics

4.2 Backlight Unit

Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	-	20	-	mA	6LEDs
Forward Voltage	V_F	18	-	19.6	V	BLH-BLL
Backlight Power Consumption	W_{BL}	-	768	-	mW	6LEDs
Operating Life Time	-	-	30,000	-	Hrs	For each LED

Note1: Figure below shows the connection of backlight LED.

B/L CIRCUIT DIAGRAM

LED;IF =20mA,VF=18-19.6V

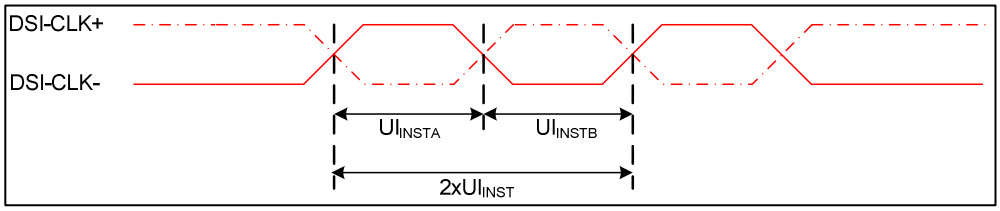
Note 2: 1LED: V_F 3.2V I_F 20mA

Note 3: I_F is defined for one LED.

Optical performance should be evaluated at Ta 25℃ only.

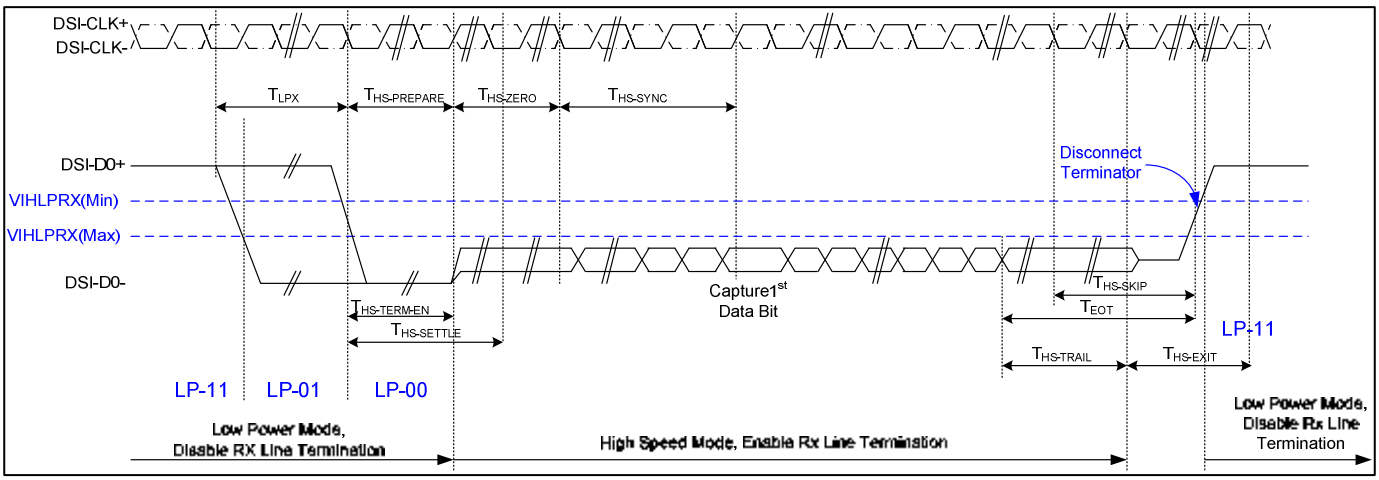
If LED is driven by high current, high ambient temperature humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50 initial brightness. Typical operating life time is estimated data.

4.3 Power Sequence



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	4	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	2	12.5	ns	

High-Speed Data Transmission

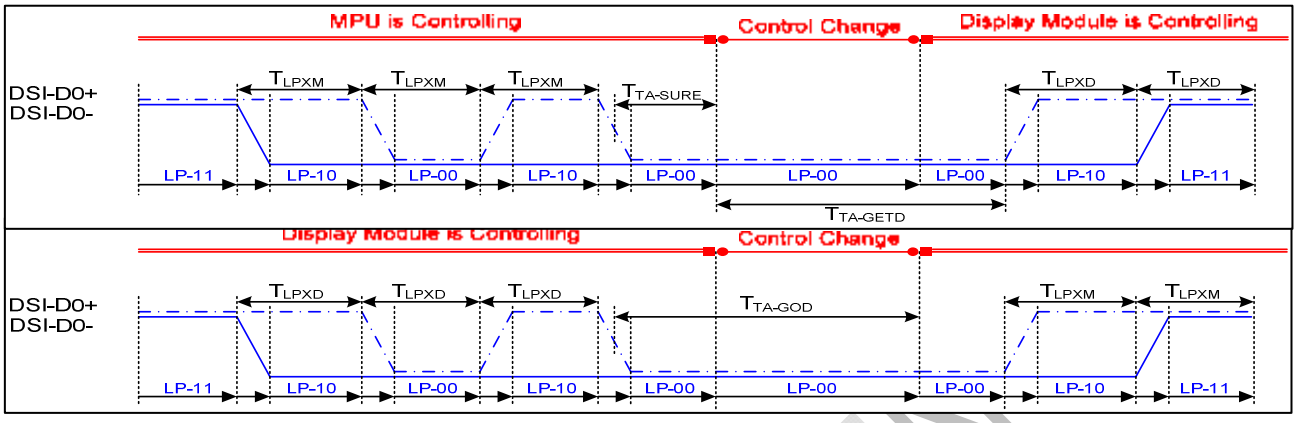


Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

5 Timing Chart

5.1 MIPI Data to clock Timing Definition

5.1.1 High Speed Mode



Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}		5 T_{LPX}		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		4 T_{LPX}		ns

High Speed Mode – Data Clock Channel Timing

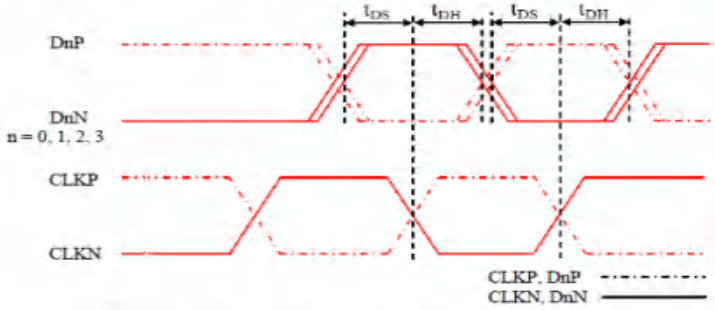


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N, n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings

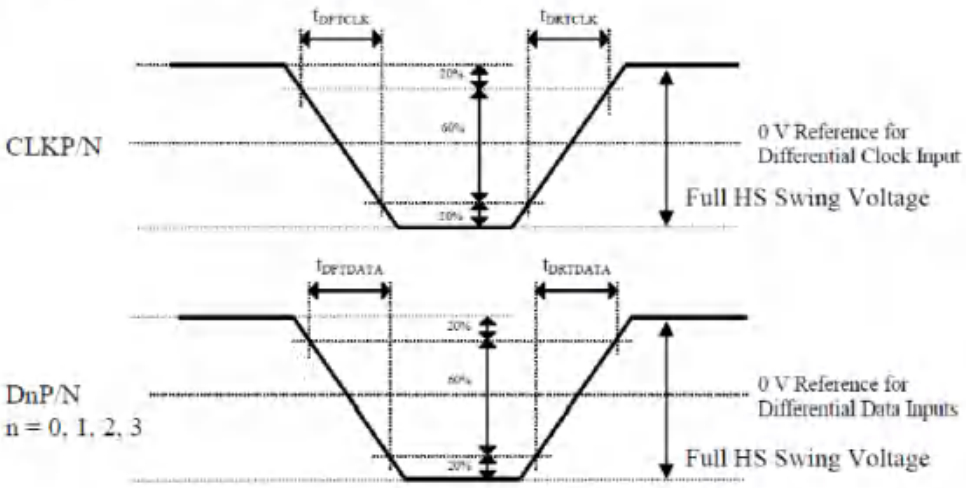


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

5.1.2 Low Speed Mode

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

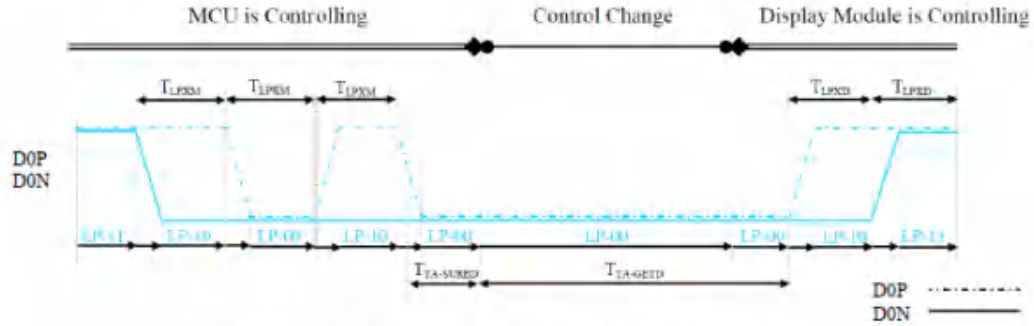


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

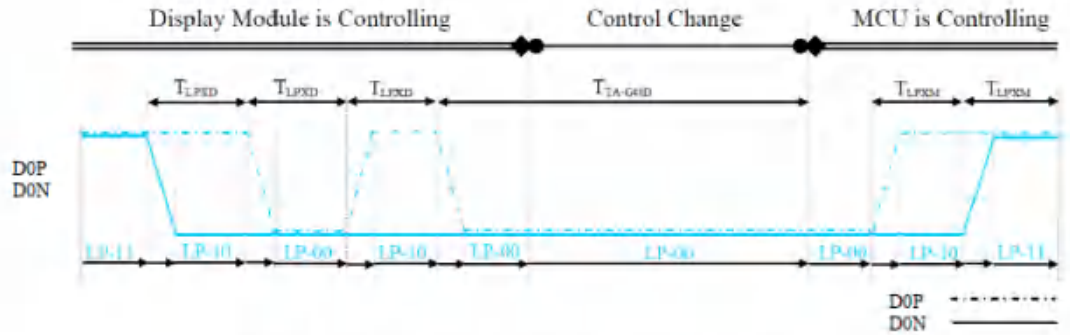


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

Data Lanes from High Speed Mode to Low Power Mode

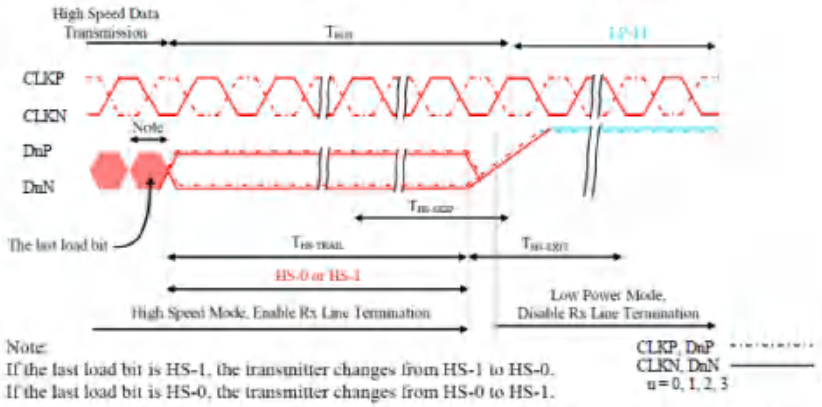


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Data Lanes from Low Power Mode to High Speed Mode

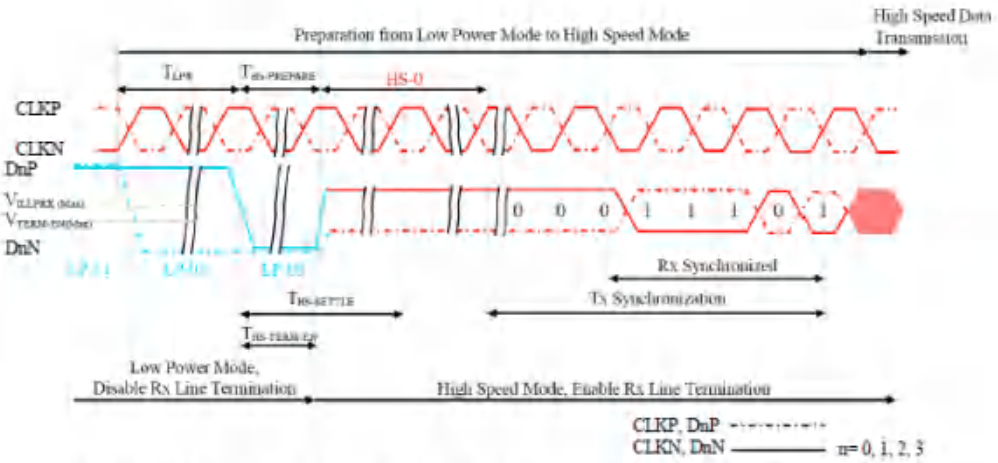


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

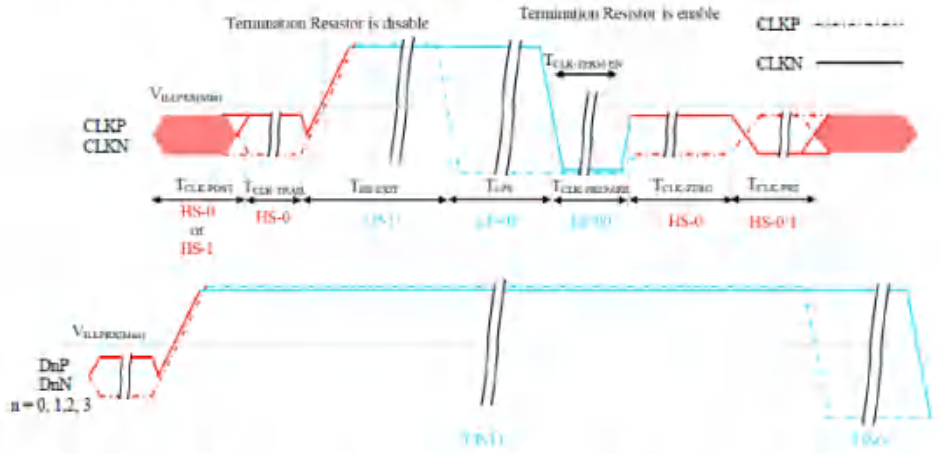
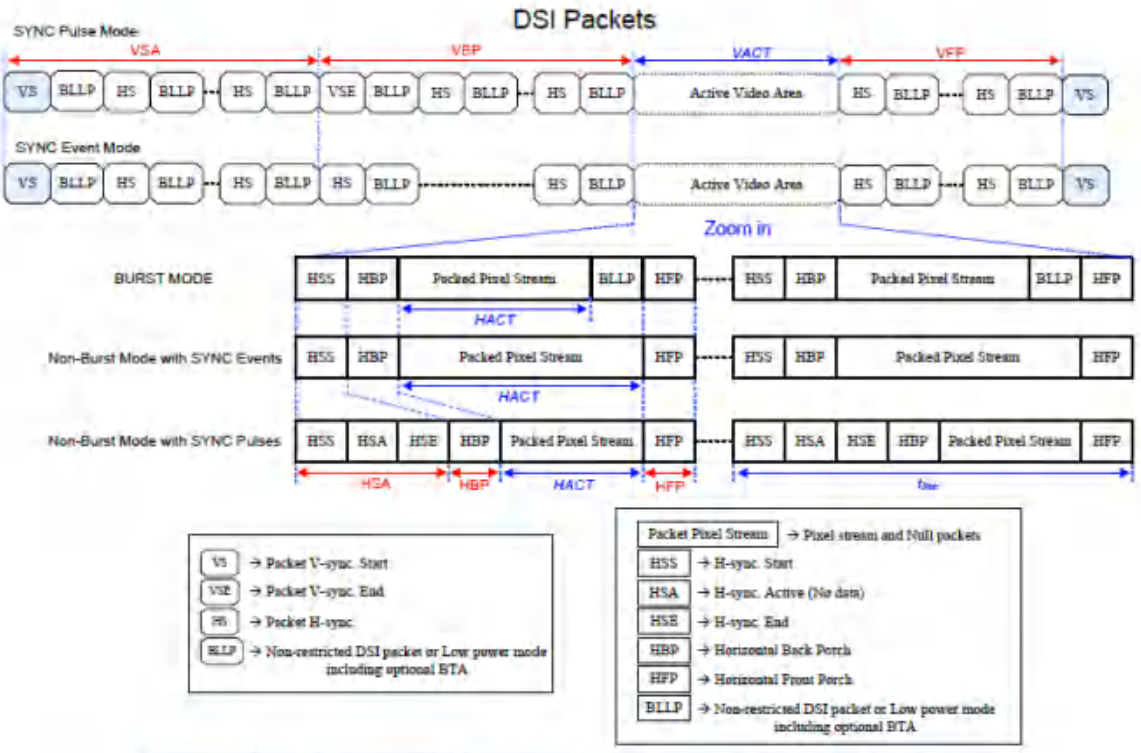


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

5.2 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{dps}	200		Note 5	Line

5.3 Reset Timing

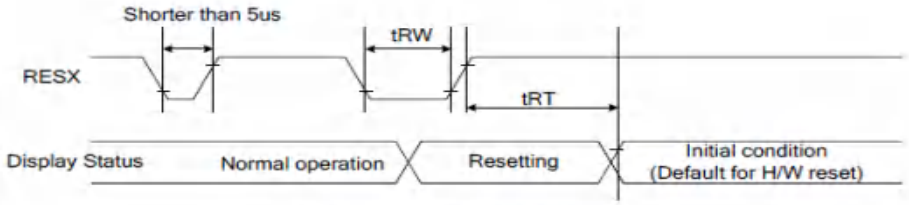


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

6 Optical Characteristics

6.1 Driving the backlight condition

Item		Symbol	Conditions	Specifications (typ)	Unit	Note
Transmittance		T%	Viewing normal angle $q_X = q_Y = 0°$	4.2	%	All left side data are based on INX's following condition – 1.CG : NTSC 69% 2.AR : 67.5% 3.Light Source : INX LED BLU 4.Machine : DMS 803 5. Vwhite > 5.0 V, Vdark < 0.3V 6. Polarizer : NPF-TEGQ1465DUHC
Contrast Ratio		CR		900	--	
Response Time		Ton+ Toff		30	ms	
Viewing Angle	Hor.	q_{X+}	Center CR>10	85	deg.	
		q_{X-}		85		
	Ver.	q_{Y+}		85		
		q_{Y-}		85		
CF only Chromaticity	Red	X_R	Viewing normal angle $q_X = q_Y = 0°$	0.290	0.320	Under C light Simulation
		Y_R		0.330	0.360	
	Green	X_G		0.661	0.691	
		Y_G		0.323	0.353	
	Blue	X_B		0.274	0.304	
		Y_B		0.583	0.613	
	White	X_W		0.134	0.164	
		Y_W		0.124	0.154	

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

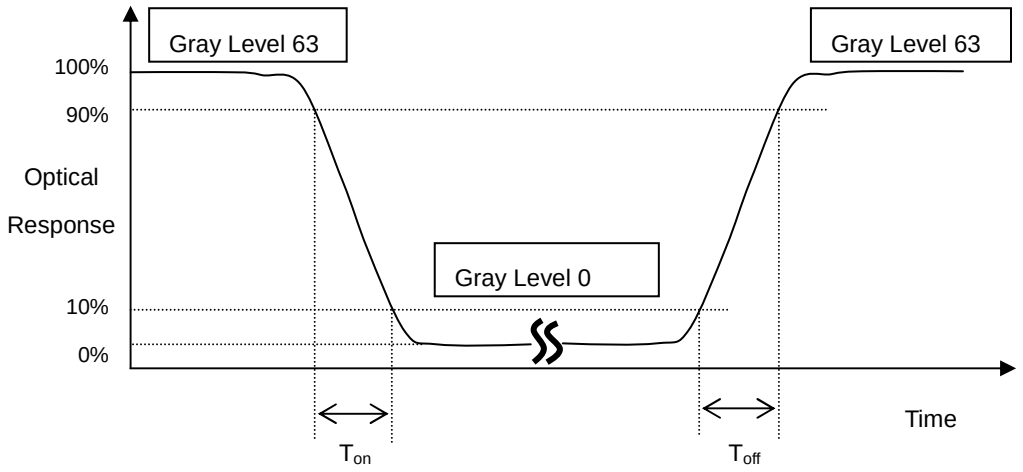
Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63

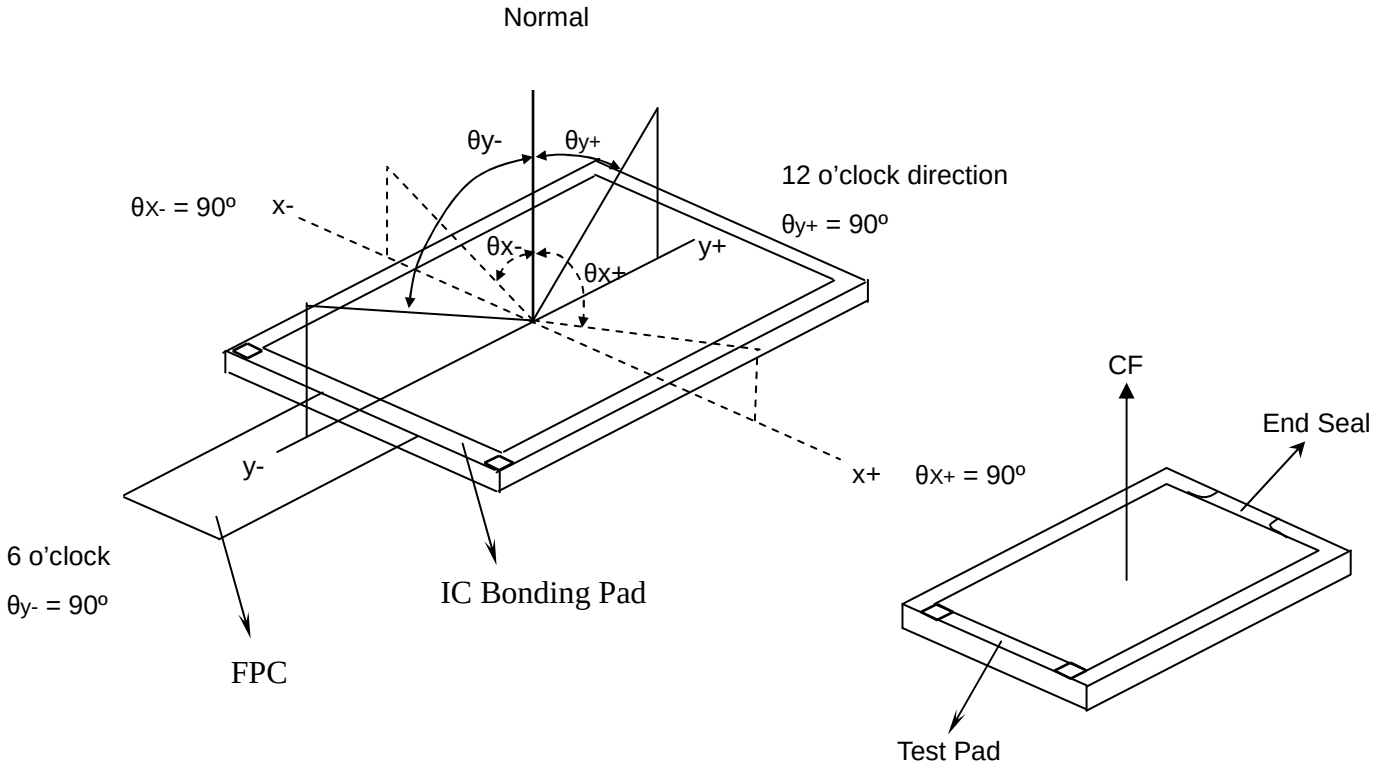
L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).



*Note(3) Definition of Viewing Angle

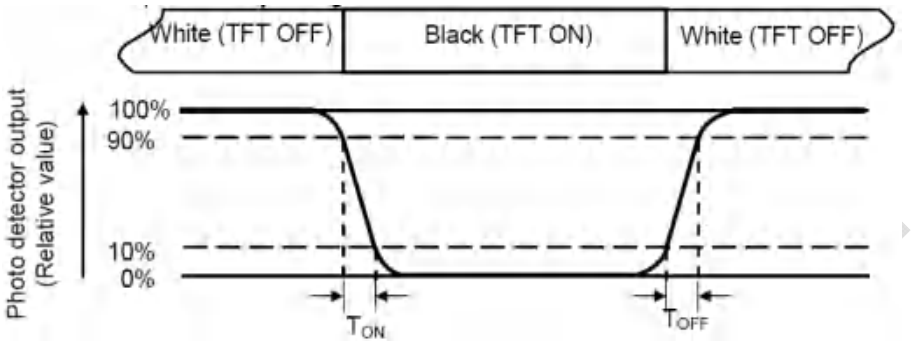


Black state : The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between White state and Black state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90 to 10 . And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10 to 90 .



Note 5: Definition of color chromaticity (CIE1931)

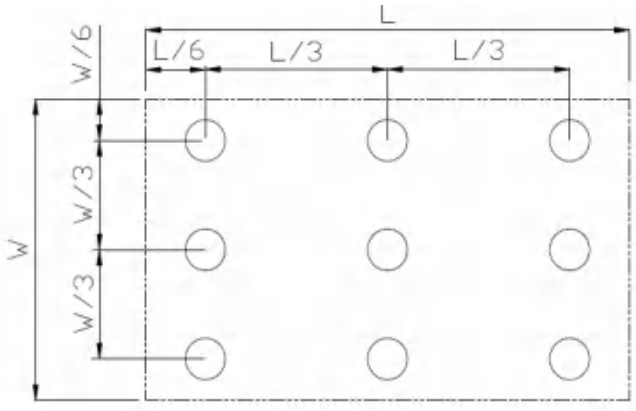
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	**Ts=+70℃, 48hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	**Ta=-20℃, 48hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	**Ta=+80℃, 48hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	**Ta=-30℃, 48hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	**Ta=+60℃, 90% RH, 48 hours Restore 2H at 25℃ Power off**	IEC60068-2-78 :2001 GB/T2423.3 2006
7	ESD Sensitivity test	**C=150pF, R=330Ω,5points/ panel Air:± 6KV, 5times, Contact:± 4KV, 5 times, （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）**	IEC61000-4-2:2001 GB/T17626.2-2006

Note1: Ts is the temperature of panel s surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

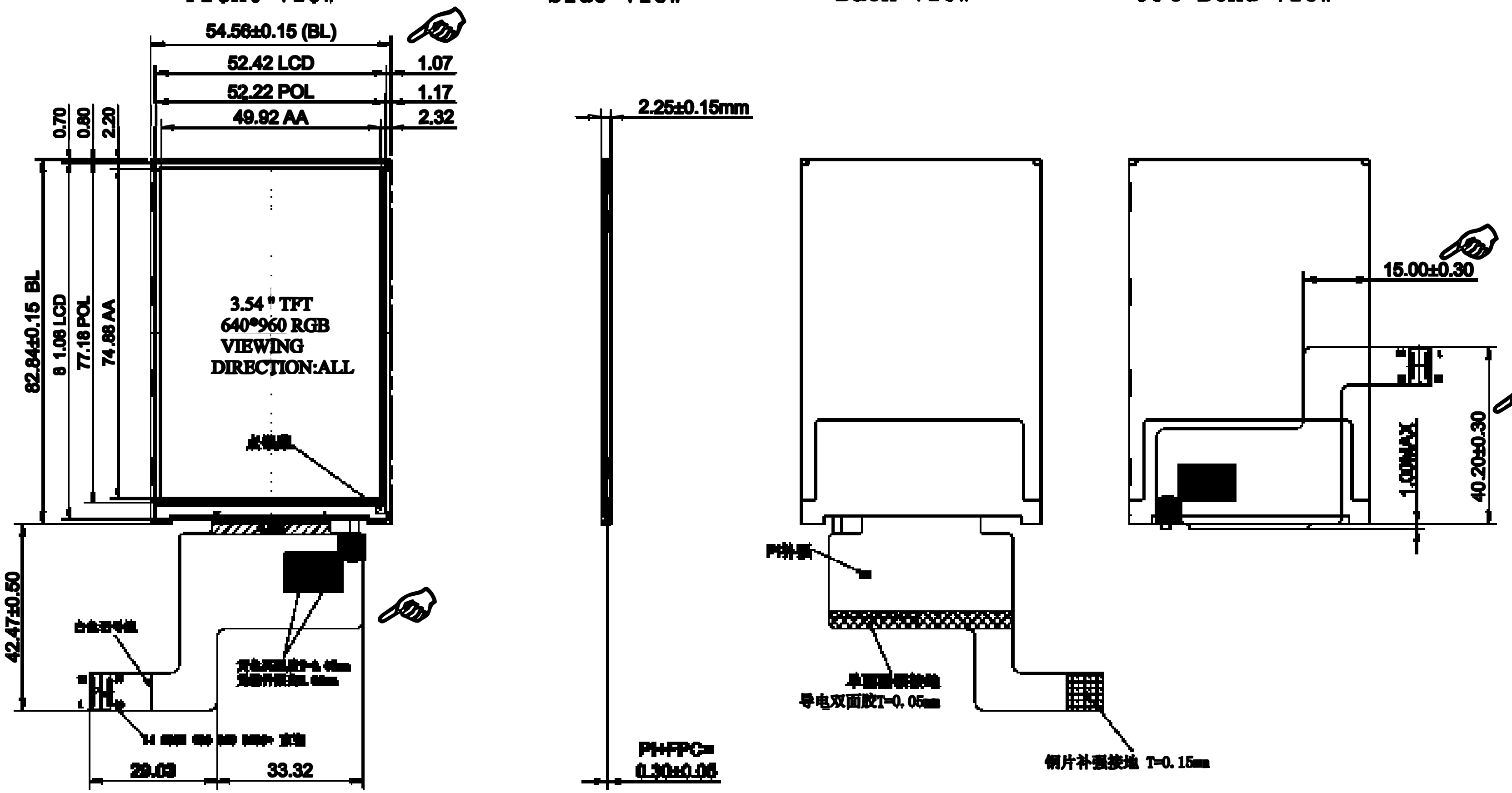
Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don t guarantee all of the cosmetic specification.

8 Mechanical Drawing

Rev.	Date	Content	Reviser
V1	2021-08-06	V0	YGP

RoHS

Front view   Side view   Back view   FPC Bend view



PIN Assignment	
1	LCD ID
2	NC
3	LEDA
4	LEDA
5	NC
6	LEDK
7	LEDK
8	NC
9	GND
10	GND
11	CLKN
12	CLKP
13	GND
14	DATA0N
15	DATA0P
16	GND
17	DATA1N
18	DATA1P
19	GND
20	GND
21	TE
22	GND
23	GND
24	LCD RST
25	NC
26	VCC(+5.0)
27	VCC(+5.0)
28	NC
29	I□VCC(1.8V)
30	I□VCC(1.8V)

NOTES:
1. Display:3.5"QVGA,ALL'clock.
2. Driver IC:ST7703
3. STORAGE TEMPERATURE:-30° C TO 80° C;
OPERATING TEMPERATURE:-20° C TO 70° C;
4. BL LED:3 CHIP-WHITE LEDS 并联, If=20*6=120mA;
5. CONNECTOR TYPE : 焊接;
6. "*" CRITICAL DIMENSION;() REFERENCE DIMENSION;
7. RECOMMENDED CELLPHONE WINDOW SIZE:0.5mm FROM LCD A.A AREA :
8. LCD warp is ≦ 0.3;
9. 偏光片：上油砂片、下增亮片.
10. 符合一级环境禁用管理物质。

B/L CIRCUIT DIAGRAM

LED;IF =20mA,VF=18-19.6V

Microtech Technology Co.Ltd.		VIEW DIRECTION THIRD ANGLE PROJECT		DRAW DATE	2021-08-06
HK Tel:(852)98152643 CN Tel:[illegible] FAX:[illegible] Http://www.microtech-lcd.com				DESIGN BY	YGP
MODULE DRAWING		UNMARK TOL	SCALE	UNIT	CHECK BY	
VERSION:	V1	±0.2	1:1	mm		
LCM NO:	MTP035DV40A-V1	PAGE 1OF 1			APPROVAL	

9 Packing Drawing

No.	Item	Model (Material)	Dimensions(mm)	Unit Weight (kg)	Quantity	Remark
1	LCM Module	MTF035DV49A-V1	54.56x82.84x2.25mm	TBD	TBD	
2	Partition	BC Corrugated paper	TBD	TBD	TBD	
3	Corrugated Paper	B Corrugated paper	TBD	TBD	TBD	
4	Corrugated Bar	B Corrugated paper	TBD	TBD	TBD	
5	Dust-Proof Bag	PE	TBD	TBD	TBD	
6	A/S Bag	PE	TBD	TBD	TBD	
7	Carton	Corrugated paper	TBD	TBD	TBD	
8	Total weight	TBD Kg±5%				

10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not sub ect it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the ad oining areas since this may cause the color tone to vary.

10.1.4 The polari er covering the display surface of the LCD module is soft and easily scratched. Handle this polari er carefully.

10.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polari er. Especially, do not use the following:

- Water
- etone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.